WE CLAIM

1. A data processing apparatus, comprising:

a dynamic node;

precharge circuitry arranged during a precharge phase to precharge the dynamic node to a first voltage level;

evaluation circuitry arranged to receive a number of input signals and during an evaluate phase to selectively drive the dynamic node to a second voltage level dependent on the input signals; and

power down drive circuitry arranged when the data processing apparatus is to enter a power down mode to drive the dynamic node to the second voltage level.

2. A data processing apparatus as claimed in Claim 1, wherein the power down drive circuitry comprises first circuitry responsive to a power down signal indicating that the power down mode is set to drive the dynamic node to the second voltage level and second circuitry responsive to said power down signal to prevent the precharge circuitry from precharging the dynamic node to the first voltage level.

3. A data processing apparatus as claimed in Claim 2, wherein the first circuitry comprises an N type device connected between the dynamic node and the second voltage level.

4. A data processing apparatus as claimed in Claim 2, wherein the second circuitry is arranged to receive the power down signal and a precharge signal indicating whether the precharge phase is active, and to generate as its output an input signal to the precharge circuitry, such that when the power down signal indicates that the power down mode is set, the output signal from the second circuitry is arranged to cause the precharge circuitry to be turned off.

5. A data processing apparatus as claimed in Claim 4, wherein the precharge circuitry comprises one or more P type devices, and said second circuitry is arranged to apply a logical OR gate function to the power down signal and the precharge signal.

6. A data processing apparatus as claimed in Claim 2, wherein the second circuitry is positioned in series with the precharge circuitry between the dynamic node and the first voltage level, the second circuitry being arranged to turn off when the power down signal indicates that the power down mode is set, thereby preventing the precharge circuitry from precharging the dynamic node to the first voltage level.

7. A data processing apparatus as claimed in Claim 1, wherein the first voltage level represents a logic 1 level and the second voltage level represents a logic 0 level.

8. A data processing apparatus as claimed in Claim 1, wherein the evaluation circuitry comprises a plurality of N type devices.

9. A data processing apparatus as claimed in Claim 8, wherein the precharge circuitry comprises one or more P type devices.

10. A data processing apparatus as claimed in Claim 1, further comprising voltage regulating circuitry arranged when the data processing apparatus is to enter the power down mode to reduce the difference between the first voltage level and the second voltage level, thereby reducing leakage current through the precharge circuitry.

11. A method of operating a data processing apparatus to reduce leakage current in a power down mode of operation, the data processing apparatus comprising a dynamic node, precharge circuitry arranged during a precharge phase to precharge the dynamic node to a first voltage level, and evaluation circuitry arranged to receive a number of input signals and during an evaluate phase to selectively drive the dynamic node to a second voltage level dependent on the input signals, the method comprising the step of:

driving the dynamic node to the second voltage level when the data processing apparatus is to enter the power down mode.

12. A method as claimed in Claim 11, wherein said driving step comprises the steps of:

(a) responsive to a power down signal indicating that the power down mode is set, causing first circuitry to drive the dynamic node to the second voltage level; and

(b) responsive to said power down signal, causing second circuitry to prevent the precharge circuitry from precharging the dynamic node to the first voltage level.

13. A method as claimed in Claim 12, wherein the first circuitry comprises an N type device connected between the dynamic node and the second voltage level.

14. A method as claimed in Claim 12, wherein said step (b) comprises the steps of:

receiving at said second circuitry the power down signal and a precharge signal indicating whether the precharge phase is active; and

generating as an output of the second circuitry an input signal to the precharge circuitry, such that when the power down signal indicates that the power down mode is set, the output signal from the second circuitry is arranged to cause the precharge circuitry to be turned off.

15. A method as claimed in Claim 14, wherein the precharge circuitry comprises one or more P type devices, and said second circuitry is arranged to apply a logical OR gate function to the power down signal and the precharge signal.

16. A method as claimed in Claim 12, wherein the second circuitry is positioned in series with the precharge circuitry between the dynamic node and the first voltage level, at said step (b) the second circuitry being arranged to turn off when the power

down signal indicates that the power down mode is set, thereby preventing the precharge circuitry from precharging the dynamic node to the first voltage level.

17. A method as claimed in Claim 11, wherein the first voltage level represents a logic 1 level and the second voltage level represents a logic 0 level.

18. A method as claimed in Claim 11, wherein the evaluation circuitry comprises a plurality of N type devices.

19. A method as claimed in Claim 18, wherein the precharge circuitry comprises one or more P type devices.

20. A method as claimed in Claim 11, further comprising the step of:

reducing the difference between the first voltage level and the second voltage level when the data processing apparatus is to enter the power down mode, thereby reducing leakage current through the precharge circuitry.

21. Selector circuitry for a memory device, comprising a data processing apparatus as claimed in Claim 1.